

A Novel Cascaded Multilevel Inverter Using A Single DC Source

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ABSTRACT: In this paper, a new structure for cascaded multilevel inverter (MLI) using a single dc source is presented. The conventional type of inverters have many issues like high total harmonic distortion (THD), non sinusoidal output, high switching stress and large number of switches. So the multilevel inverters are much popular over the conventional inverters for high voltage and high power applications. The increase in the output voltage level increases the switches and hence the control complexity. This paper presents a 25-level inverter using 10 switches and a single dc source. The input dc supply is given to the multi-output flyback converter and the output is fed to the MLI. The multi-output flyback converter requires a single switch. The proposed structure requires reduced number switches and gate driver circuit compared to the conventional MLI. The other advantages of this topology are the single dc source and reduced THD. The verification of the analytical results is carried out using MATLAB/Simulink.

KEYWORDS: BMultilevel inverter, Flyback converter, Bidirectional switch, Cascade, Phase opposition disposition SPWM, Total harmonic distortion.

I. INTRODUCTION

Multilevel inverter is a power electronic device that synthesizes a desired output voltage from several levels of dc voltages as inputs [1]. The multilevel inverter can produce a large number of output voltage levels. The staircase waveform obtained is of having better voltage capability, lower switching losses, lower harmonic distortion and high power quality. As the technology advances the multilevel inverters find useful in high power applications such as renewable energy systems, motor drives, flexible ac transmission system, industrial electric vehicle applications, fuel cells, and so on [2]-[4].

There are different types of multilevel converter topologies proposed by the researchers. Generally, multilevel converters can be classified in to neutral point clamped (NPC) [5], flying capacitor (FC) [6] and cascade H-bridge (CHB) converters [7]. According to the dc supply voltages MLI can be symmetric (equal voltages) and asymmetric (non-equal voltages) type. A good quality near sinusoidal waveform with reduced THD can be enhanced with the increased number of output levels. There is a considerable increase in the device components such as switches, dc sources, gate driver circuits etc. for these conventional types of inverters as the number of level increases. The significant increase in the number of switches increases the gate driver circuits and thereby the control complexity as well as the cost. Therefore various attempts are made by the researchers focusing on the component reduction [8]-[11]. Several modulation techniques have been developed for multilevel inverters such as fundamental frequency switching [11], carrier based pulse width modulation (PWM) [12], selective harmonic elimination [13] and space vector modulation [14]. The pulse width modulation scheme is the most efficient controlling method for the inverters. In carrier based PWM method, the reference signal is compared with the triangular carrier signal. Multicarrier PWM modulation technique is adopted in this paper. This paper proposes a novel cascaded asymmetric MLI topology with minimum number of switches which is fed by a multiple output flyback converter.

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II. RELATED WORK

An attempt has made in [9] to propose a new structure for the multilevel inverter with the reduced number of power electronic devices compared to the conventional type of cascade inverter. But this inverter requires large number of bidirectional switches and also its magnitude of blocked voltage is high. In [9] different structures of bidirectional switch combinations also explained.

In [10], another topology for cascade multilevel converter has been introduced. It reduces the number of bidirectional switches, power diodes, and dc voltage sources compared with [9]. But this topology requires large number of gate driver circuits and switches. It consists of several submultilevel converters and full-bridge converters.

R. ShalchiAlishah et al. proposed topologies for symmetric, asymmetric, and cascade switched-diode multilevel inverters in [11]. It has more advantages in comparison with the topologies in the [9], [10]. When compared with the proposed topology, it requires more number of fast recovery diodes and separate dc sources. The modulation technique used is a fundamental switching strategy, a low switching frequency compared to other control techniques. The topology [11] uses only unidirectional switches.

This paper presents a new topology for the cascaded multilevel inverter. This topology uses only a single dc source. The dc input is given to the multi-output flyback converter. The output voltage across the load of flyback converter is fed to the multilevel inverter. The flyback converter used in this structure is a single input four output converter to generate a twenty five level inverter. This multilevel requires only minimum number of power switches compared to the conventional cascade multilevel inverters.

III. BASIC UNIT OF PROPOSED MLI

The proposed topology of MLI contains minimum number of switches for generating the same number of levels as compared with the conventional types. The basic unit of MLI can generate 5 output levels using two voltage sources. Here the voltage sources represent the output voltage of the multi-output flyback converter. The proposed unit requires 4 unidirectional switches and one bidirectional switch. Several structures of bidirectional switches have been designed in [9]. This paper utilizes a bidirectional switch consists of two insulated gate bipolar transistors with an antiparallel diode. This topology uses a bidirectional switch with a common emitter configuration which requires only one gate driver circuit. The full-bridge or the H-bridge uses the unidirectional switches consists of an IGBT and an antiparallel diode. Fig. 1 shows the basic unit of MLI. The unit consists of unidirectional switches S11, S12, S13, S14 and a bidirectional switch S15. The unidirectional switches are arranged same as the conventional H-bridge while S15 is added to increase the output level by the appropriate selection of voltage source.

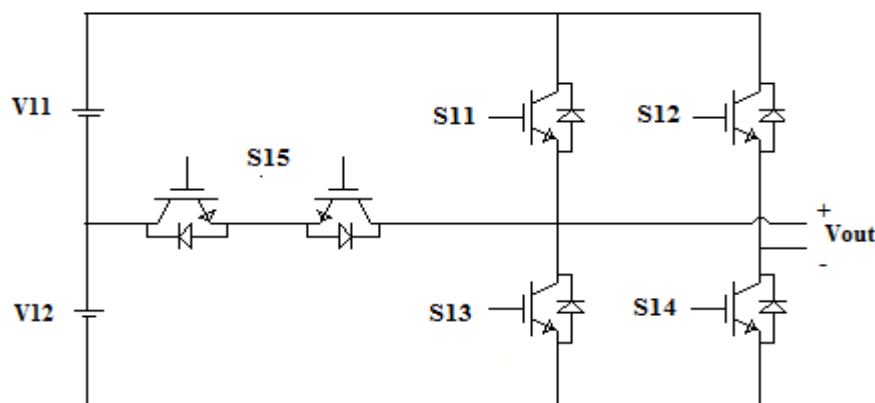


Fig. 1 Basic unit of proposed MLI

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The Table 1 shows the switching states of the basic unit of MLI. In this table, ‘1’ represents the corresponding switch in ‘ON’ state and ‘0’ represent the ‘OFF’ state. The basic unit consists of two voltage sources V11 and V12. The voltages V11 and V12 are the voltages taken across the load of (single input - two output) flyback converter.

Table 1 Switching states of basic unit

State	S11	S12	S13	S14	S15	Output Voltage (Vout)
1	1	1	0	0	0	0
2	0	0	0	1	1	V12
3	1	0	0	1	0	V11+V12
4	0	1	0	0	1	-V11
5	0	1	1	0	0	-V11-V12

The output level can be increased by increasing the number of voltage sources in the basic unit. Table 2 illustrates the relation between the output levels and the voltage sources in the basic unit. The output levels can be increased by adding the dc voltage sources and the switches. For $(2N+1)$ number of output levels the basic unit requires N number of dc sources and $(N+3)$ number of switches.

Table 2 Output levels with respect to voltage sources in the basic unit

No. of voltage sources	No. of switches	No. of output levels
2	5	5
3	6	7
4	7	9
N	N+3	2N+1

IV. MULTI-OUTPUT FLYBACK CONVERTER

The proposed topology uses a multi-output flyback converter. The single input multi output flyback converter works similar to a normal flyback converter with a multiple secondary winding transformer. Fig. 2 shows the multi-output flyback converter with a single input and four outputs. The flyback converter consists of power metal oxide semiconductor field effect transistor (MOSFET) ‘S’, diodes (D1, D2, D3, D4), multi-winding transformer for isolation purpose, ‘Lm’ magnetizing inductance, capacitors (C1, C2, C3, C4) and loads (R1, R2, R3, R4). The turns ratio of the transformer is 1:n, where ‘n’ will be different for the multiple secondary windings depending whether the

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voltage is step up or step down. The multi-output flyback converter shown in Fig. 2 has a multiple winding transformer with a single primary winding and four secondary windings with turns n_1, n_2, n_3, n_4 respectively. The number of turns decide whether the voltage to be step up or step down. The load voltage,

$$V_o = \frac{n \times V_{in} \times D}{1-D} \tag{1}$$

From equation (1), n is the turns ratio (number of secondary turns to the primary turns of the transformer) n_1, n_2, n_3, n_4 respectively for the four windings of the transformer, V_{in} is the input dc voltage, V_o is the load voltages ($V_{11}, V_{12}, V_{21}, V_{22}$ respectively) and D is the duty ratio of flyback converter.

$$D = \frac{T_{on}}{T} \tag{2}$$

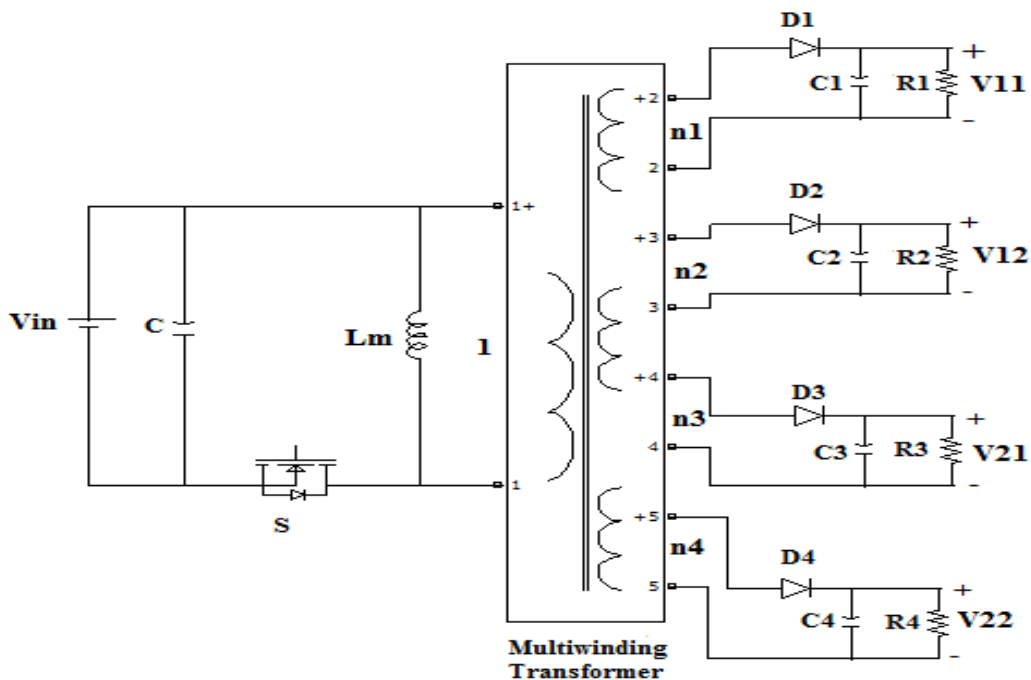


Fig. 2 Multi-output flyback converter

V. PROPOSED MLI USING FLYBACK CONVERTER

The proposed topology of MLI is employed by cascaded arrangement of two basic units. The input for the MLI is taken from the multi-output flyback converter. Fig. 3 shows a MLI with a 25 output levels using a single dc source. This arrangement can be further augmented by cascading ‘m’ number of basic unit. The increasing number of level results in near sinusoidal output waveform. The 25-level inverter consists of two cascaded basic units. Each unit consists of two equal voltage input from the flyback converter. The voltage input to the first unit to the second is in the ratio of 1:5. This topology helps to generate 25 level output. The 1:5 ratio is maintained by the proper turns ratio (1:5) in the

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transformer winding of the flyback converter. Let $n1 = n$, then $n2 = n$, $n3 = 5n$, $n4 = 5n$. This arrangement leads to an unequal voltage input to the two respective basic units (asymmetrical MLI).

$$V11 = V12 = Vdc \tag{3}$$

$$V21 = V22 = 5Vdc \tag{4}$$

$$Vm1 = Vm2 = 5^{(m-1)} \times Vdc \tag{5}$$

If 'm' number of basic units are cascaded for this particular topology then the output levels will be 5^m and the value of maximum voltage levels will be the sum of all the dc voltage input. If the voltage inputs to the cascaded units are equal that is 1:1 ratio, then the arrangement is said to be a symmetrical MLI.

$$V11 = V12 = V21 = V22 = Vm1 = Vm2 = Vdc \tag{6}$$

This arrangement would generate $(4m+1)$ output levels and the maximum output voltage level is $(2m \times Vdc)$.

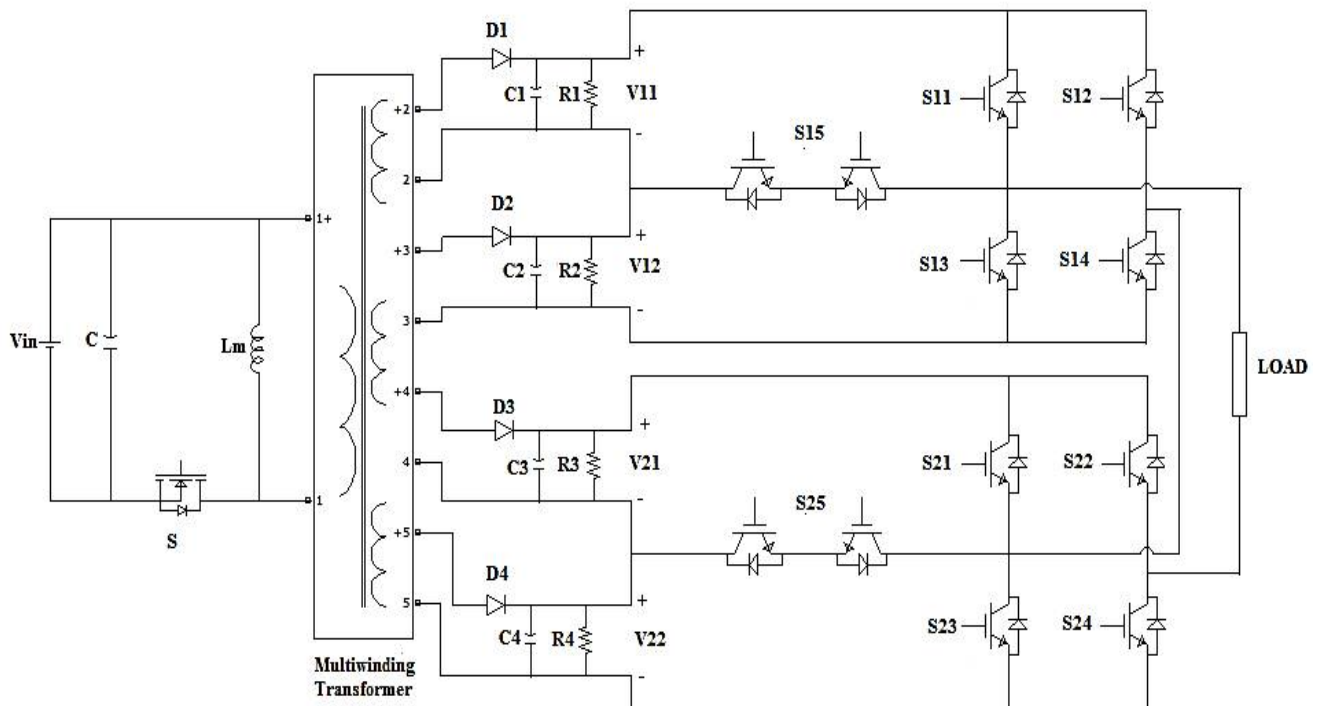


Fig. 3 Proposed 25 level inverter using a multi-output flyback converter

The proposed structure requires a multi-output flyback converter and a 25-level inverter. The output of the flyback inverter is fed to the MLI. It requires 10 switches for the MLI and one switch for the flyback converter for its operation. The input to the MLI is taken across the loads R1, R2, R3 and R4 of the flyback converter.

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VI. OPERATION OF PROPOSED STRUCTURE

The proposed MLI uses a single input four output flyback converter. The flyback converter is operated by using a single dc source. The duty ratio of the switch ‘S’ is selected according to the output voltages needed. The operation of multi-output flyback converter is similar to the conventional single input single output flyback converter. The transformer windings also depend on the load voltages. The operation of the proposed MLI is illustrated in the Table 3. The load voltage V11, V12, V21 and V22 of the flyback converter is fed to the MLI respectively. The logic ‘1’ is considered as the ‘ON’ state and logic ‘0’ is considered as the ‘OFF’ state of the switch. The switches S15 and S25 are the selection switches to add the number of output levels. The basic units are connected in series to form cascade structure. The output of each basic unit is added together to achieve the final output voltage.

Table 3 Switching states of proposed 25-level inverter

State	S11	S12	S13	S14	S15	S21	S22	S23	S24	S25	Output Voltage
1	1	1	0	0	0	1	1	0	0	0	0
2	0	0	0	1	1	0	0	1	1	0	V12
3	1	0	0	1	0	0	0	1	1	0	V11+V12
4	0	1	1	0	0	0	0	0	1	1	V22-V12-V11
5	0	1	0	0	1	0	0	0	1	1	V22-V11
6	0	0	1	1	0	0	0	0	1	1	V22
7	0	0	0	1	1	0	0	0	1	1	V22+V12
8	1	0	0	1	0	0	0	0	1	1	V22+V12+V11
9	0	1	1	0	0	1	0	0	1	0	V22+V21-V12-V11
10	0	1	0	0	1	1	0	0	1	0	V22+V21-V11
11	0	0	1	1	0	1	0	0	1	0	V22+V21
12	0	0	0	1	1	1	0	0	1	0	V22+V21+V12
13	1	0	0	1	0	1	0	0	1	0	V22+V21+V12+V11
14	0	1	0	0	1	0	0	1	1	0	-V11
15	0	1	1	0	0	0	0	1	1	0	-V12-V11
16	1	0	0	1	0	0	1	0	0	1	V12+V11-V21
17	0	0	0	1	1	0	1	0	0	1	V12-V21
18	0	0	1	1	0	0	1	0	0	1	-V21
19	0	1	0	0	1	0	1	0	0	1	-V11-V21
20	0	1	1	0	0	0	1	0	0	1	-V12-V11-V21
21	1	0	0	1	0	0	1	1	0	0	V12+V11-V22-V21
22	0	0	0	1	1	0	1	1	0	0	V12-V22-V21
23	0	0	1	1	0	0	1	1	0	0	-V22-V21
24	0	1	0	0	1	0	1	1	0	0	-V11-V22-V21
25	0	1	1	0	0	0	1	1	0	0	-V12-V11-V22-V21

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The multilevel converters can be controlled by using different modulation schemes [11]-[14]. For this topology a multicarrier PWM technique is adopted [15]. The carrier based PWM technique is used to generate the switching pulses for the MLI. In this technique the sinusoidal reference signal is compared with the triangular carrier waveform. In this topology phase opposition disposition sinusoidal PWM (POD SPWM) is adopted for its simplicity and all the carrier waveforms are in phase with each other as shown in Fig. 4. The pulses obtained are used for switching the MLI corresponding to the respective voltage levels.

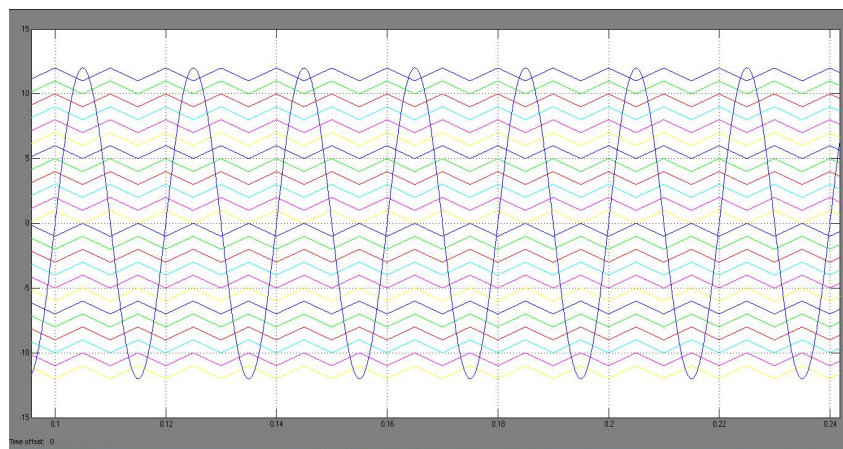


Fig. 4 POD SPWM technique

VII. SIMULATION RESULTS

The simulink model of the proposed 25 level inverter using a single source is shown in Fig. 5. The simulations are performed using MATLAB. The simulink model mainly consists of the multilevel inverter circuit, subsystem for the pulses generation and subsystem for the multi-output flyback converter. The load used for the system is an R-L load.

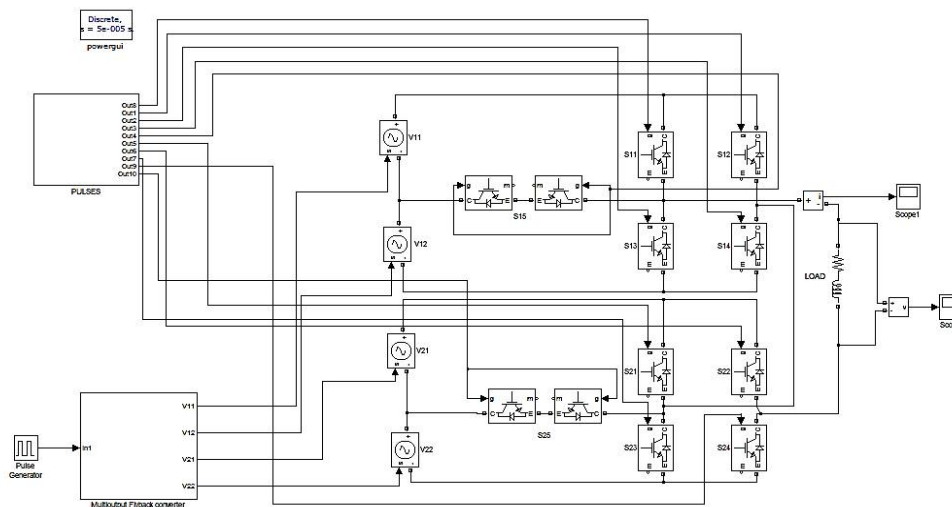


Fig. 5 Simulink model of proposed structure

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The subsystem of POD SPWM and multi-output flyback converter is shown in Fig. 6(a) and 6(b) respectively. Fig. 6(a) shows the POD SPWM simulation. In this modulation technique all the twenty four carriers are compared with the sine waveform. For all the carrier waveforms above the time-axis, the results of comparison with the reference sine wave are '1' or '0'. For all the carrier waves below the time-axis, the results of comparison with the reference sine wave are '0' or '-1'. The signals so obtained are aggregated so as to synthesize an aggregated signal 'As'. The aggregated signal has same number of output levels as desired in the output waveform. The switching signals are derived from this 'As' by comparing the signal with the desired level using the lookup table and the output is fed to the switches of MLI. The lookup table is generated by using the switching states of the 25-level inverter. The fig. 6(b) is the subsystem for the multi-output flyback converter. It provides a single input and four outputs using a multiple winding transformer. The output of this flyback converter is connected to the MLI.

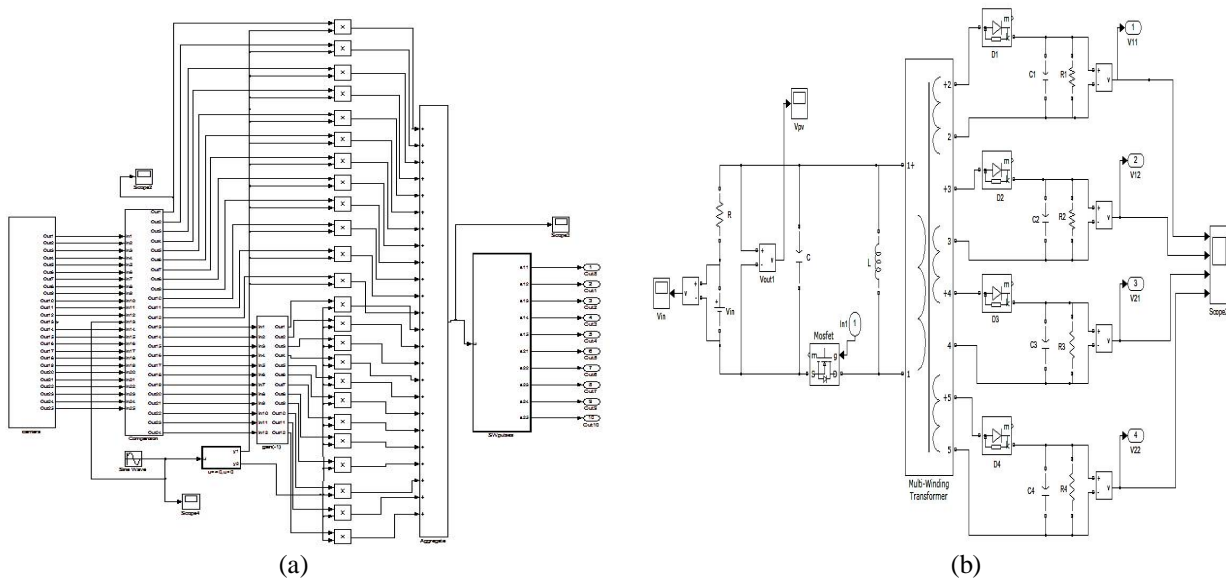


Fig. 6 Subsystem of (a) POD SPWM and (b) multi-output flyback converter

The load used in the MLI is an R-L load with $R = 10\Omega$ and $L = 1\text{mH}$. The input supply given to the flyback converter $V_{in} = 50\text{ V}$ dc supply, then the output obtained is of a 25-level inverter with a maximum voltage of 100V across the load with a 50Hz frequency. The output of the flyback converter is $V_{11} = V_{12} = 9\text{V}$ and $V_{21} = V_{22} = 41\text{V}$. The output voltage obtained is shown in Fig.7. The maximum output voltage obtained in this structure is the sum of the load voltages of the multi-output flyback converter. The output voltage is composed of twenty five levels.

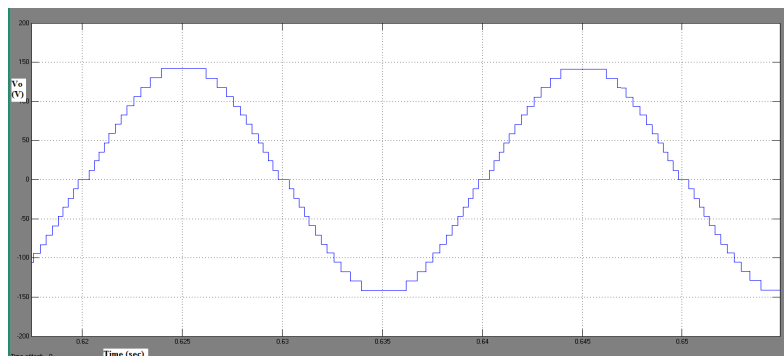


Fig. 7 Output voltage of proposed 25-level inverter

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The gate pulse to the switches in the MLI is shown in Fig. 8. The multilevel inverter requires 10 switches for twenty five level output. The pulses generated are by using the POD-SPWM technique. The corresponding pulses are given to switches S11, S12, S13, S14, S15, S21, S22, S23, S24 and S25 respectively in the Fig. 8. The resulting total harmonic distortion of the proposed structure is shown in Fig. 9. The THD of this structure is 4.31%. The total harmonic distortion is very less compared to conventional cascade inverters.

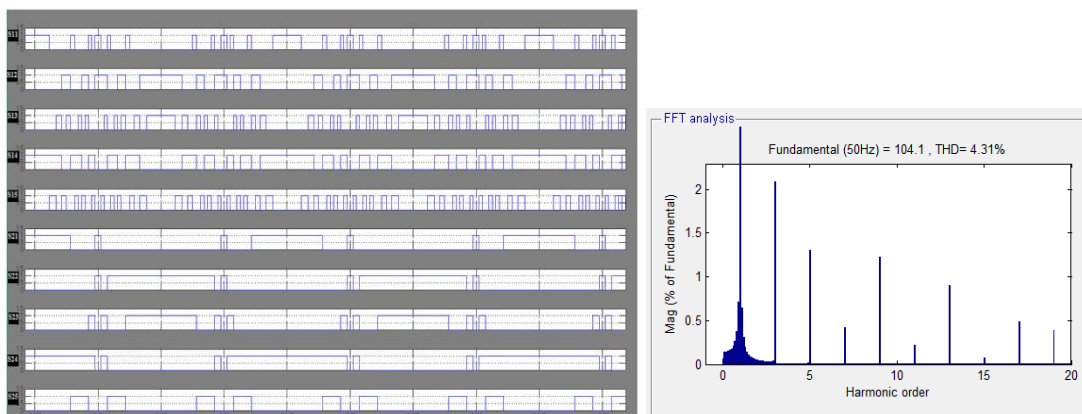


Fig. 8 Gate pulses of the proposed modulation scheme

Fig. 9 THD of 25-level inverter

VIII. CONCLUSION

A novel cascaded multilevel inverter topology using a single dc source is proposed in this paper. Compared with the conventional multilevel inverters, it requires less number of switches to achieve same number of output levels. The low THD value results in a good quality near sinusoidal output waveform. The structure and principle of operation of the proposed topology is detailed. The POD-SPWM modulation technique used in this structure is also explained. Since proposed structure uses only a single dc source, it is applicable in renewable energy sources, fuel cells, motor drive applications etc. The operations of the cascaded MLI using the flyback converter have been verified by MATLAB software.

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BIOGRAPHY



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